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EXAMINER	
WANG, TED M	
ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,067	WALSH ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-11* is/are allowed.

6)☒ Claim(s) *1-5,7 and 12-15* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments and amendments, filed on 3/22/2007, with respect to claim 1-7 and 12-14 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments and amendments, filed on 3/22/2007, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claim 15

(1) *Applicants' argument* – "The design of the Keaveney et al. produces an output signal with a resultant phase which is phase locked to the input reference signal for channels at the same frequency. One drawback of the design of Keaveney et al. is that it cannot be programmed to vary phase of the output signal with respect to the phase of the input reference signal as claimed by applicants." as recited in page 14 of remark, dated 3/22/2007.

Examiner's response –

Column 3, lines 34-59 of Keaveney's references teaches that each time phase locked loop 12 is switched to a different channel, for example, interpolator being reset, that is, the frequency of its output, f_{OUT}, is changed by changing any one or more of the parameters F, M, N, the balancing process starts anew. In addition, Keaveney further teaches that in fractional-N synthesizers the higher

frequency output signal f_{OUT} is only in phase with the input reference frequency 28 every M periods of the reference signal. That is, during the phase locked processing the phase of said output signal will be varied with respect to the phase of said input reference signal, f_{REF}.

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(e) with Keaveney's reference is adequate.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 13 is rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art of the instant application.

- With regard claim 13, the admitted prior art of the instant application teaches a method of varying the phase of the output signal with respect to the input reference signal of a fractional-N synthesizer (Fig.1 element 10), the method comprising the steps of:

  tracking an accumulated fractional phase (Fig.1 element F, M, interpolator 26, F/M, where the interpolator could be an accumulator (page 3 lines 8-9));

  scaling (Fig.1 element 24) the accumulated fractional phase by a predetermined phase value (Fig.1 element N); and

  loading the predetermined phase value into an interpolator to define a predetermined output frequency and phase (Fig.1 element 22).

5. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Keaveney et al. (US 6,556,086 B2).

- With regard claim 15, Keaveney et al., cited by the instant applicant, discloses a method of varying the phase of the output signal with respect to the input signal of a fractional-N synthesizer (Fig.1 element 10), the method comprising:

  generating a synchronization pulse (Fig.1 element 40) at integer multiples of periods of the input reference signal (Fig.1 element 28 and column 2 lines 26-33);

  generating a predetermined phase adjustment value (Fig.1 elements F, M, and F/M, column 1 lines 46-51, where F is the input fraction and M is the Modulus and both F and M are predetermined, column 1 lines 47-51); and

generating an enable signal (Fig.1 elements 46 and 44 and column 4 lines 1-18) to reset (Fig.1 element 48 and column 4 lines 1-18) an interpolator (Fig.1 element 26) of said fractional-N synthesizer with said predetermined phase to vary the phase of said output signal with respect to said input reference signal (column 3 lines 35-59, where the frequency of its output, f_{OUT}, is changed by changing any one or more of the parameters F, M, N and received input frequency, since it is phase locked to the input frequency. Refer to Response to Arguments as addressed in the above paragraph.)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 7, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art of the instant application in view of Staszewski et al. (2002/1091727).

- With regard claim 1, the admitted prior art of the instant application teaches a fractional-N synthesizer (Fig.1 element 10) with programmable output phase comprising: a phase locked loop (Fig.1 element 12) having an output signal whose frequency is a fractional multiple of an input reference signal (equations 1

and 2), said phase locked loop including a frequency divider (Fig.1 element 20); a synchronization circuit (Fig.1 element 40) responsive to said input reference signal for generating synchronization pulses at integer multiples of M periods of said input reference signal (page 11 lines 17-23); an interpolator (Fig.1 element 26) responsive to F and M, where F is a fractional value and M is the modulus, to provide to said frequency divider an output which is a fractional value equal to, on average, said an input fraction F/M (page 10 lines 17-21).

The admitted prior art of the instant application discloses all of the subject matter as described in the above paragraph except for specifically teaching a phase adjustment circuit responsive to said synchronization circuit for varying the phase of said output signal with respect to said input reference signal.

However, Staszewski et al. teaches a phase adjustment circuit (Fig.5 elements 38, 64a, 64b, adder and multiplexer) responsive to said synchronization circuit (Fig.5 elements 64a, 64b, 66 and R/F (rising and falling control signal, which is synchronized to the FREF) and paragraph [0040]) for varying the phase of said output signal with respect to said input reference signal (paragraphs 43-50) in order to increase the timing updated for the phase locked loop so that the great accuracy could be obtained (paragraph 11, lines 14-17). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the phase adjuster (Fig.5 elements 38, 64a, 64b, adder and multiplexer) as taught by Staszewski et al. in which responsive to said synchronization circuit for varying the phase of said output signal with respect to

said input reference signal, into Fig.1 between f_{REF} 28 and interpolator 26 input F of the admitted prior art of the instant application so as to improve the PLL accuracy.

- With regard claim 2, the modified circuit of the admitted prior art of the instant application and Staszewski et al. further disclose said phase adjustment circuit includes a switching circuit (Fig.1 element Multiplexer with R/F control signal, where R/F represents rising/falling control signal with respect to the f_{REF}, paragraph [0040], Staszewskis' reference) for selectively applying said fractional value (Fig.5 element 64a output) and said a modified fractional value (Fig.5 output of the adder with one input connected Frac(ΔΦ), Staszewskis' reference) to said interpolator (Fig.1 element 26 of the admitted prior art of the instant application) to define a predetermined phase relationship between said output signal and said input reference signal.
- With regard claim 3, the modified circuit of the admitted prior art of the instant application and Staszewski et al. further disclose said switching circuit includes an adder circuit for adding said fraction value and a predetermined phase adjustment value to define said modified fractional value (Fig.5 output of the adder with one input connected Frac(ΔΦ), Staszewskis' reference).
- With regard claim 4, the modified circuit of the admitted prior art of the instant application and Staszewski et al. further disclose said switching circuit includes a multiplexer configured to select said modified fractional value or said fractional value for one or more reference cycles (Fig.1 element Multiplexer with R/F

control signal, where R/F represents rising/falling control signal with respect to the f_{REF}, paragraph [0040], Staszewskis' reference).

- With regard claim 5, the modified circuit of the admitted prior art of the instant application and Staszewski et al. further disclose said fractional value is offset by a phase word to define said modified fractional value (Fig.5 element Frac($\Delta\Phi$).
- With regard claim 7, which is a fractional-N synthesizer claim related to claim 1, the modified circuit of the admitted prior art of the instant application and Staszewski et al. further disclose a phase register including a predetermined phase adjustment value (Fig.5 elements 64a/64b, Fig.6 element 94 and paragraph 51). All other limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 12, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 14, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

8. Claims 8-11 are allowed.

9. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang

DAC HA
PRIMARY EXAMINER